

Product Brief

Intel® 3100 Chipset

Embedded Computing



Intel® 3100 Chipset for Embedded Computing

Product Overview

The Intel® 3100 chipset combines server-class memory and I/O controller functions into a single component, creating the first integrated Intel® chipset specifically optimized for embedded, communications, and storage applications. When combined with Intel® Pentium® M or Intel® Celeron® M processors on 90nm process technology, the Intel 3100 chipset addresses developers' needs for high-performance, high-reliability, low-power platforms within small form-factors such as PrAMC, CompactPCI* and COM Express*.

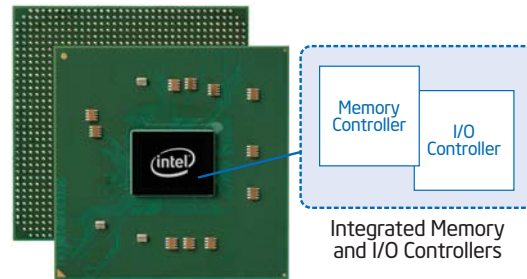
PCI Express* serial I/O technology and DDR2 memory technology increase I/O bandwidth and reduce system latency for data-intensive applications. The 400 to 667 MHz front-side bus (FSB) provides support for Intel Pentium M and Intel Celeron M processors, as well as an upgrade path to future use with next-generation Intel® dual-core processors. The Intel 3100 chipset includes a four-channel Enhanced Direct Memory Access (EDMA) controller, providing low-latency, high throughput data transfer capability with no CPU intervention for higher overall system performance. It also integrates I/O controller features such as Serial ATA, PCI and USB, saving board real-estate and power by removing the need for a separate, legacy I/O bridge chip.

Along with a strong ecosystem of hardware and software vendors, including members of the Intel® Communications Alliance (intel.com/go/ica), Intel helps cost-effectively meet development challenges and speed time-to-market.

Product Highlights

PCI Express

For demanding I/O and networking applications, PCI Express interfaces attach a variety of Intel and third-party I/O solution components and adapters directly to the Intel 3100 chipset (one x8 PCI Express interface, and one x4 PCI Express interface). Each interface may be bifurcated to provide additional configuration flexibility. The PCI Express interfaces provide throughput speeds of up to 4 GB/s on the x8 interface, and up to 2 GB/s on the x4 interface, allowing I/O to keep pace with the rest of the platform.



Memory

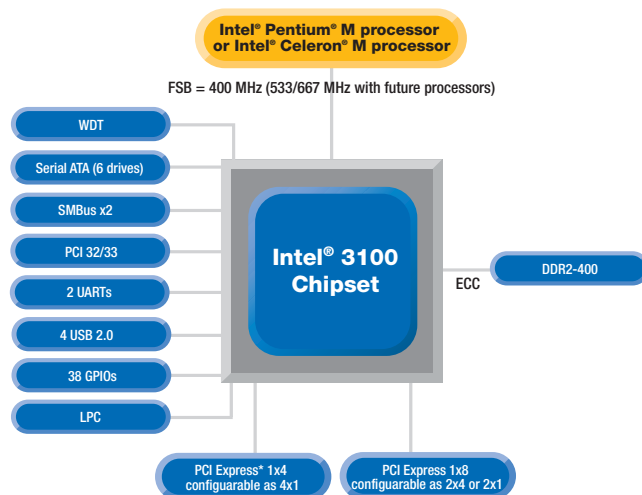
Intel 3100 chipset-based platforms support single-channel DDR2-400 memory (up to 4 GB with Intel Pentium M and Intel Celeron M processors). DDR2-400 memory technology is ideal for storage and memory-intensive applications, providing up to 10% increase in memory bandwidth and up to 40% decrease in power consumption over DDR 333. The memory subsystem interface supports up to four ranks for a total system bandwidth of 3.2 GB/s.

Data Protection

The Intel 3100 chipset is designed to bring enterprise-level reliability, availability, serviceability, usability and manageability (RASUM) to the embedded platform. The FSB supports parity, and all internal buses are supported by 2-bit parity. The PCI Express interface supports 32-bit cyclic redundancy check (CRC) for detection and automatic recovery of transient signaling errors. Memory interface supports Single Error Correct/Double Error Detect (SEC/DED) ECC, auto retry on uncorrectable errors, and integrates a hardware memory scrubber to scan the populated memory space, proactively seeking out soft errors in the memory subsystem.

Enhanced Direct Memory Access (EDMA)

A four-channel EDMA controller efficiently moves data within local system memory or from the local system memory to the I/O subsystem. Each EDMA channel provides low-latency, high-throughput data transfer capability with no CPU intervention for higher overall system performance. These transfers may be individually designated to be coherent (snooped on the FSB) or non-coherent (not snooped on the FSB), providing improvements in system performance and utilization when cache coherence is managed by software rather than hardware. EDMA also enables Quality of Service (QoS) by prioritization of data.



Features

Supports Intel® Pentium® M and Intel® Celeron® M processors on 90nm process

40 mm x 40 mm FC-BGA package

PCI Express*

DDR2-400 memory interface

Advanced Platform RAS

GPIO

USB 2.0

Two UARTs (Serial Port)

32/33-bit PCI Bus Interface

SMBus x2

Integrated Serial ATA Host Controllers

Watchdog Timer

Power Management

Benefits

- Optimized performance for multiple market segments and price points, supporting a range of processor frequencies (from 1.0 GHz to 1.8 GHz) and power constraints (from 5.5W to 21 W TDP). Specific processors supported include: Intel® Pentium® M processor 745^A (1.8 GHz) 2 MB L2 Cache; Intel® Pentium® M processor Low Voltage 738^A (1.4 GHz) 2 MB L2 Cache; Intel® Celeron® M processor Ultra Low Voltage 373^A (1.0 GHz) 512 KB L2 Cache; Intel® Celeron® M processor 370^A (1.5 GHz) 1 MB L2 Cache.

- Requires 50% less board space than prior-generation two-chip chipsets¹

- Direct connection between the Intel® 3100 chipset and PCI Express component/adapters; bandwidth up to 4 GB/s on the x8 PCI Express interface; higher bandwidth and less I/O bottlenecks than PCI-X*

- Maximum memory bandwidth of 3.2 GB/s
- Decreased power consumption – especially important on dense rack, hot-plug controller and blade configurations

- Memory ECC, SEC/DED, and DIMM scrubbing can improve system reliability
- 32-bit CRC on PCI Express
- Hot swap PCI Express enhances serviceability
- SMBus port hooks for remote management operation and support for a variety of third-party base management controller and BIOS solutions

- 38 pins (25 dedicated, 13 mux'ed)

- One USB 2.0 host controller with a total of four ports
- Supports wakeup from sleeping in S3 and S5 states

- Two full-function 16550-compatible serial port UARTs

- Supports PCI Rev 2.3 specification at 33 MHz
- Supports two request/grant pairs

- First SMBus dedicated as slave; second configurable as master or slave

- Six ports provide independent DMA operation
- Supports SATA 1.0a or AHCI mode

- Multiple modes (WDT and free-running)

- ACPI 2.0 support

Product	Product Code	Thermal Design Power	Package
Intel® 3100 Chipset	LE3100MICH	10.4 – 12.4W	1284 Flip Chip-Ball Grid Array (FC-BGA3)

¹Comparison with Intel® E7520 Memory Controller Hub plus Intel® 6300ESB I/O Controller Hub

^AIntel processor numbers are not a measure of performance. Processor numbers differentiate features within each processor family, not across different processor families. See http://www.intel.com/products/processor_number for details.

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO SALE AND/OR USE OF INTEL PRODUCTS, INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT, OR OTHER INTELLECTUAL PROPERTY RIGHT. INTEL MAY MAKE CHANGES TO SPECIFICATIONS, PRODUCT DESCRIPTIONS, AND PLANS AT ANY TIME, WITHOUT NOTICE.

Intel Corporation may have patents or pending patent applications, trademarks, copyrights, or other intellectual property rights that relate to the presented subject matter. The furnishing of documents and other materials and information does not provide any license, express or implied, by estoppel or otherwise, to any such patents, trademarks, copyrights, or other intellectual property rights. Intel products are not intended for use in medical, life saving, life sustaining, critical control or safety systems, or in nuclear facility applications. The Intel® 3100 Chipset may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are available upon request.

Intel, the Intel logo, Intel. Leap ahead., Intel. Leap ahead. logo, Pentium, and Celeron are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

*Other names and brands may be claimed as the property of others.

Copyright © 2006 Intel Corporation. All rights reserved.

Printed in USA

0506/KSC/OCG/XX/PDF

♻ Please Recycle

313126-001US

